The Folding Dickson Converter: A Step Towards Fully Integrated Wide Input Range Capacitive DC-DC Converters

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***Abstract*—This paper presents a novel approach to wide input range capacitive DC-DC converters. The star connected Dickson converter is used, not only for its low bottom plate voltage swing and efficient use of switches, but also for its very regular structure. This regular structure allows it to operate as a folding Dickson converter, implementing several conversion ratios, as well as reusing all of its flying capacitance. Folding is achieved by changing the phases of the switches, and keeping certain flying switches on in both phases, virtually lumping flying capacitors together. This last fact, along with the other benefits of the Dickson converter, makes it a good candidate for full integration. The flying switches of the converter are driven from their own converter, using an adapted bootstrapped converter which uses the intrinsic operation of the Dickson converter to copy the voltage of the flying capacitors and boost it by V_{out}.**

I. Introduction

For years inductive buck converters have dominated the scene of switched-mode power supplies, due to their theoretical efficiency reaching 100% and being able to operate over wide input voltage ranges. Attempts have been made to fully integrate inductive power converters [2], which has shown that the low quality on-die inductors severely limit the achievable efficiency. Using an external or in-package inductor both increase the form factor and bill of materials, which is not acceptable for many applications.

Recent developments in the field of capacitive DC-DC converters have shown that these converters can not only outperform their inductive counterpart [4], but are readily fully integrated in a standard CMOS process [3] [6]. In [1] it is shown that both capacitors and switches are used more efficiently in capacitive DC-DC converters, since they only see a fraction of the input voltage, and need conduct only a fraction of the output current, leading to a low $G{\cdot}V^2$, and are as such efficiently used. On the other hand, the switches in an inductive Buck converter need to block the entire input voltage and be able to conduct the entire output current, leading to a high $G \cdot V^2$ product, and will as such need very large devices with higher voltage capabilities such as DMOS switches. Furthermore, switches and capacitors are both efficiently implemented in CMOS processes, capable of achieving moderate to high efficiencies. With the advent of trench capacitors, efficiencies of 90% and more can be achieved at power densities of several $W's/mm^2$ [5].

A disadvantage of switched capacitor converters, is the bound on theoretical efficiency. For a single topology, the efficiency of the converter can never be higher than $\gamma = \frac{V_o}{V_{in} \cdot VCR}$. This means that frequency control of the converter is often limited to a narrow range to keep the efficiency at an acceptable level. To alleviate the constraint on theoretical efficiency, gearbox converters are often implemented [3] [6]. However,these converters usually have a fairly limited range ($\sim 1 \cdot V_{out}$), or, in the case of [4], use external capacitors and bridge part of the converter to achieve several conversion ratios. This can not be motivated in a fully integrated solution, where turning off part of the converter will lead to an unacceptable increase in switching frequency, especially for low conversion ratios. To this end, this paper proposes to use the star connected folding Dickson converter, which allows the use of several conversion ratios and reuse of all of the flying capacitors. The system overview can be seen in figure 1. In section II, the basic operation of the converter is discussed. Section III goes into more detail of the implementation of the converter core, and section IV shows the measurement results.

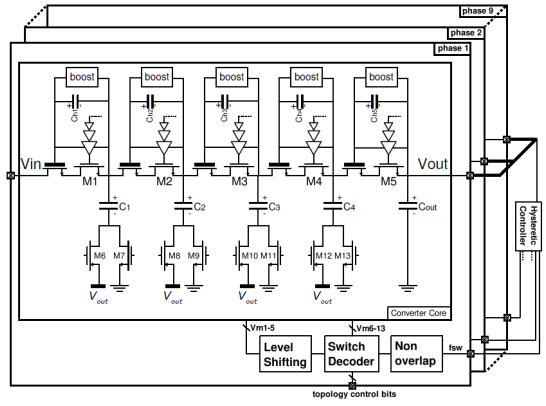

Fig. 1. System overview of the folding Dickson Converter

II. Folding Dickson Converter

The basic folding operation will be explained using Figure 2, which shows the converter core and two possible switching schemes. In its standard operation, both bottom plate phases ($M_{6-8-10-12}$ and $M_{7-9-11-13}$) and flying switches (M_{1-5}) phases alternate, realizing a 1/5 conversion ratio. To realize another conversion ratio, such as a 1/2 conversion ratio, it suffices to switch the bottom plates in the same phase, and keeping switches $M_2 - M_4$ on in both phases. This virtually lumps all the flying capacitors together, altering the topology but using all of the flying capacitors to transfer charge, and

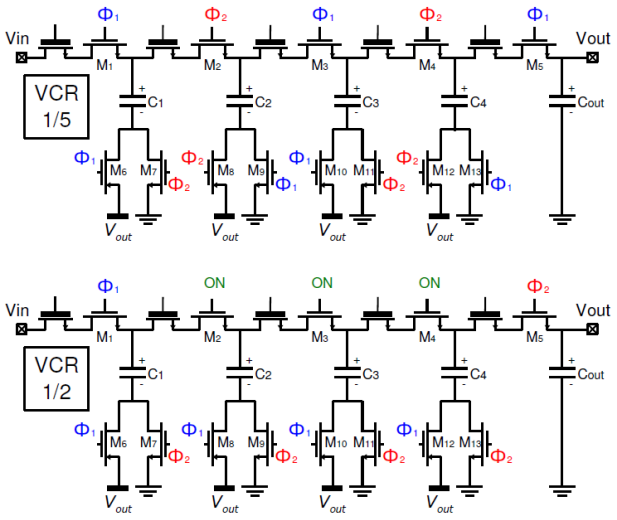

Fig. 2. The converter core and two possible switching schemes, realising a $\frac{1}{5}$ and a $\frac{1}{2}$ conversion ratio.

thus keeping the switching frequency low. Since this operation and the required circuits are very regular, the concept can be extended to more than 4 flying capacitors. The cost to implement a folding converter becomes clear when writing down the charge multiplier vectors of the 1/2 converter from figure 2:

$$a_c = [\frac{1}{8}, \frac{1}{8}, \frac{1}{8}, \frac{1}{8}] \tag{1a}$$

$$a_r(\phi_1) = [\frac{4}{8}, \frac{3}{8}, \frac{2}{8}, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0] \tag{1b}$$

$$a_r(\phi_2) = [0, \frac{1}{8}, \frac{2}{8}, \frac{3}{8}, \frac{4}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}] \tag{1c}$$

Leading to the following K_c and K_s metrics:

$$K_c = (\sum_{i=1}^{4} a_c[i])^2 = 1/4; \; K_s = (\sum_{i=1}^{13} a_r[i])^2 = 12.25 \tag{2}$$

If we compare this to a standard $1C_{fly}$ 1/2 converter, we see that the K_c is unaltered, and K_s is about three times larger for this specific case. This is due to switches M_{1-4}/M_{2-5} being connected in parallel in ϕ_1/ϕ_2. However, since M_{2-4} need to conduct in both phases, there is no need to switch their gates, hence mitigating the dynamic losses. A comparison between the original converters' and the folding dickson converter's K_c and K_s metrics are shown in table I.

Topology	K_c	K_s	K_c F.D.	K_s F.D.
$\frac{1}{2}$	$\frac{1}{4}$	4	$\frac{1}{4}$	12.25
$\frac{1}{3}$	$\frac{4}{9}$	5.44	$\frac{4}{9}$	9
$\frac{1}{4}$	$\frac{9}{16}$	6.25	$\frac{9}{16}$	7.56
$\frac{1}{5}$	$\frac{16}{25}$	6.76	$\frac{16}{25}$	6.76

TABLE I: K_c and K_s metrics for the standard topology and the Dickson converter using 4 flying capacitors

To further motivate the use of the folding Dickson converter, a comparison will be made between the losses of a 1/2 converter using only a fourth of the total flying capacitance (i.e. part of the converter is disabled or bridged), and the losses of a 1/2 folding dickson converter with the full amount of flying capacitors. Both the parasitic gate losses P_{gate} as the parasitic capacitance losses $P_{C_{par}}$ (i.e. the losses accounted the swing on the parasitic capacitors between bottom plate and ground) will be expressed in function of a required R_{SSL} and R_{FSL}, which define the output impedance of the converter.
Assume a total capacitance of C_{tot} and an equal scaling of C_{1-4}, according to the charge multiplier vector. Since we require a 1/2 operation, only $\frac{C_{tot}}{4}$ is used in the bridging case, and as such the slow switching impedance R_{SSL} can be written as:

$$R_{SSL} = \frac{K_c}{fsw \cdot \frac{Ctot}{4}} \tag{3}$$

The bottom plates of the flying capacitors undergo a swing of $\Delta V_{bp} = V_{out}$, and the parasitic capacitance from bottom plate to ground can be written as αC_{fly}. This allows us to write down the dynamic losses of the flying capacitors in function of the required R_{SSL}:

$$\begin{aligned} P_{C_{par}} &= \alpha \cdot f_{sw} \cdot \frac{C_{tot}}{4} \cdot \Delta V_{bp}^2 \\ &= \alpha \cdot \frac{\frac{1}{4}}{R_{SSL} \cdot \frac{C_{tot}}{4}} \frac{C_{tot}}{4} \cdot V_{out}^2 \\ &= \frac{\alpha \cdot V_{out}^2}{4 \cdot R_{SSL}} \end{aligned} \tag{4}$$

For the folding Dickson converter, the total amount of flying capacitance C_{tot} is used, resulting in:

$$\begin{aligned} P_{C_{par}} &= \alpha \cdot \frac{\frac{1}{4}}{R_{SSL} \cdot C_{tot}} \cdot C_{tot} \cdot V_{out}^2 \\ &= \frac{\alpha \cdot V_{out}^2}{4 \cdot R_{SSL}} \end{aligned} \tag{5}$$

This first result shows us that both approaches are identical in terms of dynamic losses of the parasitic capacitances of the flying capacitors, for a given R_{SSL}. The same result is observed when these losses are written down for other conversion ratios of the Dickson converter.
A similar approach can be used to compare the dynamic losses of the switches. The fast switching impedance can be written as:

$$R_{FSL} = \frac{2 \cdot K_s}{Gtot} \tag{6}$$

with G_{tot} the summed conductance of all switches and $K_s = 4$ (see table I) in the bridging case. Assuming all switches are scaled according to the charge multiplier vector, and one type of switch is used with technology parameters K_n the transconductance parameter, V_t the threshold voltage, and L the minimal gate length, each switch in the bridging 1/2 converter requires the following width W for a given R_{FSL}:

$$W_{1-4} = \frac{2 \cdot L}{R_{FSL} \cdot Kn \cdot (V_{gs} - V_t)} \tag{7}$$

The gate losses can then be written as following, filling in f_{SW} and W_{1-4} from eq. (3) and (7):

$$\begin{aligned} P_{gate} &= 4\, W_{1-4}\, L\, C_{sq}\, f_{sw}\, V_{gs}^2 \\ &= 4 \cdot \frac{2\, L^2\, C_{sq}\, V_{gs}^2}{K_n\,(V_{gs} - Vt) R_{SSL}\, R_{FSL}\, C_{tot}} \end{aligned} \tag{8}$$

with C_{sq} the linearized gate capacitance per area. A similar deduction leads to the following sizings for folding dickson switches, with $K_s = 12.25$ (see table I):

$$W_{1-5} = \frac{4}{28} \frac{2\, K_s\, L}{R_{FSL}\, K_n (V_{gs} - V_t)} \tag{9a}$$

$$W_{6-13} = \frac{1}{28} \frac{2\, K_s\, L}{R_{FSL}\, K_n (V_{gs} - V_t)} \tag{9b}$$

As said earlier, switches M_{2-4} are kept on in both phases, resulting in no gate losses for these switches. As in eq. (8), the gate losses can be written as:

$$\begin{aligned} P_{gate} &= 2 \cdot P_{gate,1-5} + 8 \cdot P_{gate,6-13} \\ &= 2 \cdot \frac{4 \cdot 12.25}{28} \frac{2\, L^2\, C_{sq}\, V_{gs}^2}{K_n\,(V_{gs} - Vt) R_{SSL}\, R_{FSL}\, C_{tot}} \\ &+ 8 \cdot \frac{1 \cdot 12.25}{28} \frac{2\, L^2\, C_{sq}\, V_{gs}^2}{K_n\,(V_{gs} - Vt) R_{SSL}\, R_{FSL}\, C_{tot}} \\ &= 1.75 \cdot \frac{2\, L^2\, C_{sq}\, V_{gs}^2}{K_n\,(V_{gs} - Vt) R_{SSL}\, R_{FSL}\, C_{tot}} \end{aligned} \tag{10}$$

This shows that the folding Dickson converter outperforms a Dickson converter that uses bridging or disabling part of its core, by more than a factor 2. A similar deduction can be made for the other conversion ratios, although the difference in parasitic gate losses will be less pronounced.

Beside this obvious advantage in parasitic gate losses, other factors might prohibit the large increase in switching frequency, giving favor to the folding Dickson approach. Furthermore, when changing the output tap of the converter, as in [4], the upper part of the converter that is not transferring charge to the output is still operational, which would lead to an increase in parasitic capacitance losses as well.

III. Implementation Considerations

The converter core consists of 4 flying capacitors and 13 switches, as shown in Figure 1. Switches M_{6-13} see only $1 \cdot V_{out}$, so it suffices to implement these switches using core voltage devices. In the theoretical optimum ($\gamma = \frac{V_{out,eff}}{V_{out,ideal}} = 1$), switches $M_1 - M_5$ see only $2 \cdot V_{out}$, encouraging the use of I/O-devices, capable of withstanding voltages up to 2.5V. However, when the input voltage increases for constant output voltage within one topology (using on-chip hysteretic frequency control), the blocking voltage increases, and a single I/O-device no longer suffices. Using a cascode of a standard voltage device and an I/O device, over $3 \cdot V_{out}$ can be blocked, while still achieving a better $R_{on}/area$ than for a cascode of two I/O devices. The biasing voltage of the I/O-cascode is used from the floating 1.2V supply, whose circuit is shown in Figure 3.

This circuit operates synchronously to the main converter, and uses the intrinsic operation of the Dickson converter to generate a floating rail of 1.2V for each of the flying switches, similar to an approach used in [7]. In the first phase, assuming

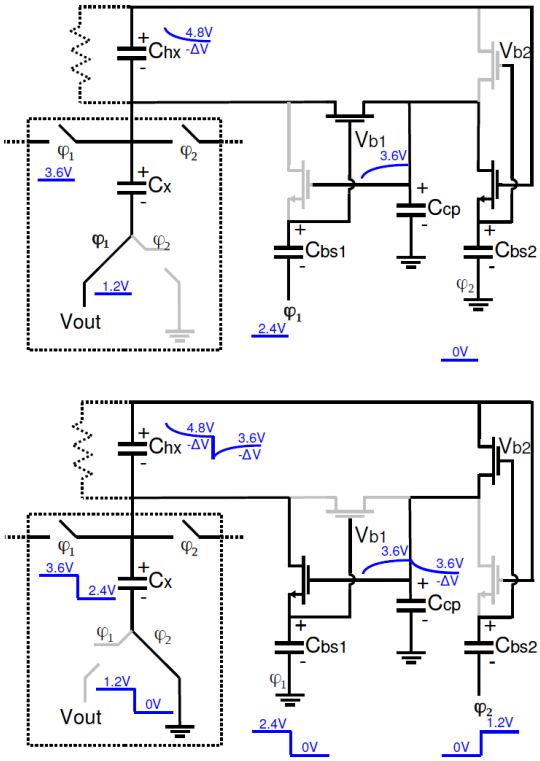

Fig. 3. Two phase operation of the bootstrapped gate boost converter.

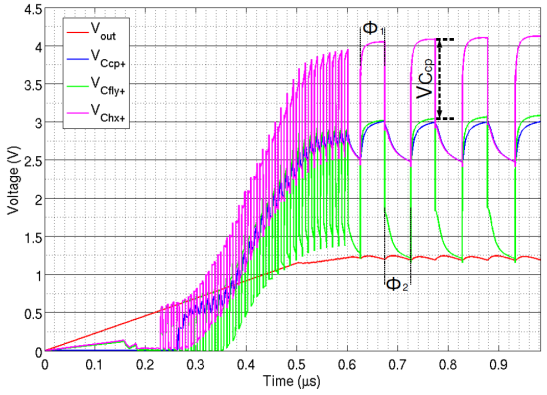

Fig. 4. Start up and nominal behaviour of the bootstrapped gate circuit, from simulation.

C_{bs1} has been precharged to V_{Cx}, M1 is turned on by bootstrap capacitor C_{bs1}, and C_{cp} is charged to $V_{Cx} + V_{out}$. In the next phase, the flying capacitor's bottom plate is connected to ground, and the top plate voltage drops by V_{out}. At this instant, M2 is turned on using bootstrap capacitor C_{bs2}, and capacitor C_{hx} is charged by capacitor C_{cp}. Since C_{cp} has been charged with a voltage $V_{Cfly} + V_{out}$, and the bottom plate of C_{hx} (i.e. top plate of C_{fly}) is connected to a potential of V_{Cfly}, the capacitor C_{hx} is effectively charged to V_{out}, or 1.2V, providing a floating rail to drive floating switches $M_1 - M_4$ and bias their cascodes.

Furthermore, the inherent nature of this bootstrapped gate circuit allows the converter to start up with no additional circuitry in the converter core required. The only requisite is

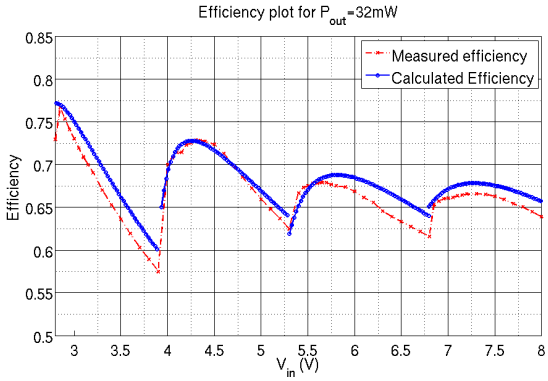

Fig. 5. Measured versus calculated efficiency for an output power of 32mW.

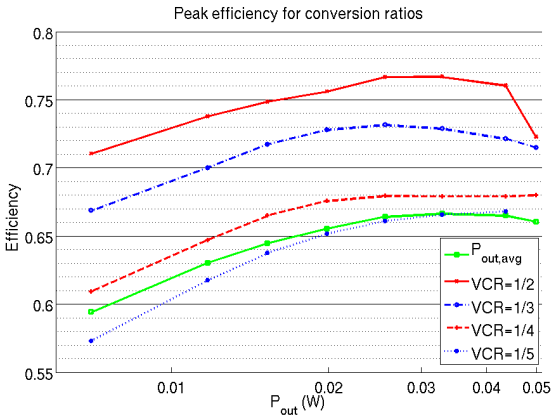

Fig. 6. Peak efficiency over P_{out} for each topology, and the average efficiency over the V_{in} range for each output power.

the availability of the output voltage, which can be provided by e.g. a linear regulator at start up. The start up behaviour of this circuit is shown in figure 4, as well as its nominal operation.

IV. Measurements and Conclusion

The Folding Dickson converter has been implemented in a 90nm technology, using a 9-phase interleaved hysteretic controller as shown in Figure 1. The chip micrograph can be seen in Figure 7. The efficiency of the converter core has been measured for constant output voltage and varying input voltage, covering a range from 2.8V to 8V. Frequency control is used in each topology for 1.2V input voltage variation. The measurements are performed over 1 decade, from 50mW to 5mW. The efficiency for one power point can be seen in Figure 5, compared to the calculated efficiency. As can be seen, the results are a close match to the predicted efficiencies.
Figure 6 shows the peak efficiency for each topology over the entire power range, and the average efficiency for each output power. As can be seen, the 1/2 conversion ratio achieves fairly high peak efficiency ($\sim 75\%$). At the worst case, for an input voltage of 4V, the efficiency is still close to 60%, due to a γ of 0.6, as can be seen in Figure 5. A comparison with the state-of-the-art is made in table II.

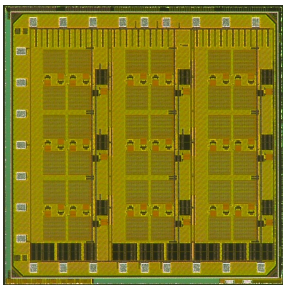

Fig. 7. Chip micrograph of the 9-phase interleaved Folding Dickson Converter

Work	[3]	[6]	This work
Topologies	$\frac{4}{5}\cdot\frac{2}{3}$	$\frac{2}{5}\cdot\frac{1}{3}$	$\frac{1}{2}\cdot\frac{1}{3}\cdot\frac{1}{4}\cdot\frac{1}{5}$
Capacitors	MIMCAP	3.88nF MOSCAP	2nF MIMCAP
Power density	$1.51mW/mm^2$	$190mW/mm^2$	$16.3mW/mm^2$
η_{peak}	88%	74.3%	77%
Voltage range	$V_{out} = [0.5 - 0.85]V$ $V_{in} = [0.7 - 1.2]V$	$V_{out} = 1V$ $V_{in} = [3 - 4]V$	$V_{out} = 1.2V$ $\mathbf{V_{in} = [2.8 - 8]V}$

TABLE II: Comparison with State-of-the-Art

V. Conclusion

This paper discusses the implementation of the folding Dickson converter, a novel, very modular approach to wide input range capacitive DC-DC converters. The converter achieves high efficiency ($\sim 75\%$) in the low input voltage range, and maintains a reasonable efficiency over the entire input voltage range of $\sim 4 \cdot V_{out}$. The use of the Dickson converter topology, which has a very attractive bottom plate swing and can be folded to achieve several conversion ratios with full reuse of all capacitors, is as such a good candidate for full integration of wide input range capacitive DC-DC converters. Thanks to its very regular structure and operation, the concept can easily be extended to implement more voltage conversion ratios.

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